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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/656,551 | 09/06/2000 | Zheng Zhang | 10991625-1 | 9625 |

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EXAMINER

PUENTE, EMERSON C

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2184

DATE MAILED: 04/25/2003

3

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/656,551

Applicant(s)

ZHANG ET AL.

Examiner

Emerson C Puente

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 September 2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☒ Claim(s) 7-9 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

DETAILED ACTION

1. Claims 1-9 have been examined.

Claim Objections

2. Claim 2 is objected to because of the following informalities:

In regards to claim 2, "said memory"(line 3 of claim) lacks antecedent basis.

Appropriate correction is required

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,079,030 of Masubuchi in view of Applicant's Admitted Prior Art, referred hereinafter "AAPA".

In regards to claim 1, Masubuchi discloses a computer system comprising:

an application memory organized as a plurality of cache lines, each cache line being identified by an address (see figure 10 item 26 and figure 1-3 item 32 and column 1 line 56-57 and column 3 lines 20-25 and column 6 lines 40-49);

a buffer for storing a plurality of cache lines (see figure 10 item 28 and figure 1-3 item 33 and column 1 lines 49-53).

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a central processing unit (CPU) for executing instructions stored in said application memory (see figure 10 item 10 and figure 1-3 item 30 and column 1 lines 56-57 and column 2 lines 35-36);

a state memory for storing the contents of the internal registers of said CPU (see column 2 lines 55-58);

a checkpoint controller for defining a series of repeating checkpoint cycles, said checkpoint controller having access to a plurality of registers in said CPU that defines the state of that CPU at a point in each of said checkpoint cycles that is controllable by said checkpoint controller(see column 2 lines 13-24); and

a memory controller for operating said application memory and said buffer, said memory controller receiving a cache line from said CPU in response to a write command specifying an address A in said application memory at which said cache line is to be stored, wherein a copy of said cache line as stored in said application memory at address A, is copied into said buffer upon receiving the first write command specifying A after the start of the current checkpoint cycle, said cache line received in said write command replacing the contents of A in said application memory (see column 1 lines 59-65).

However, Masubuchi fails to disclose a FIFO buffer.

AAPA disclose a computer system that uses a FIFO buffer to reconstruct the state of a slave computer's memory to the last checkpoint (see page 1 lines 27-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to use a FIFO buffer. A person of ordinary skill in the art would have been motivated to make the modification to Funahashi because Funahashi disclose a buffer for retaining the preceding state of the memory and a FIFO buffer, as per teaching of AAPA, constitutes a buffer, which can be used to retain the preceding state of the memory.

In regards to claim 2, Masubuchi discloses a computer system wherein each checkpoint cycle comprises a computational phase and a checkpoint phase. Masubuchi discloses write processing from the processor, indicating a computational phase (see column 1 lines 59-60) and further discloses the act of storing the contents of the main

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memory and the internal state of the processor, indicating a checkpoint phase (see column 2 lines 12-24);

and wherein said checkpoint controller during said checkpoint phase causes said CPU to write back to said memory all dirty cache lines and to store internal registers defining the state of said CPU in said memory. Masubuchi discloses at the time of a checkpoint the internal states of the processor, which constitute as internal registered defining the state of said CPU in said memory and the updated data item held in the cache, which constitute dirty cache lines, are written back to main memory(see column 3 lines 20-25).

In regards to claim 3, Masubuchi fails to disclose wherein the checkpoint controller empties the contents of the FIFO buffer at the end of the checkpoint phase if no error has been detected by the end of the checkpoint phase.

However, AAPA discloses wherein the checkpoint controller empties the contents of the FIFO buffer at the end of the checkpoint phase if no error has been detected by the end of the checkpoint phase.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to empty the contents of the FIFO buffer at the end of the checkpoint phase if no error has been detected by the end of the checkpoint phase because upon determination at the end of the checkpoint phase there is not error, it is determined that content in the memory are valid and, thus, there is no need of the information of the FIFO buffer. By emptying the contents of the FIFO buffer, one is able to free up space for the next cycle.

In regards to claim 4, Masubuchi discloses a computer system wherein said checkpoint controller, in response to a determination that a processing error has occurred, copies the contents of said buffer into said application memory, causes said CPU to copy the contents of said state memory into said CPU's internal registers, and restarts said computer system. Masubuchi discloses to bring the main memory into the preceding state, the memory control section reads and writes the data from the before image buffer (see column 2 lines 4-8), indicating copies the contents of said buffer into said application memory. He further states performing a checkpoint at suitable time

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intervals and storing the internal states of all of the processors, it is possible to return control from any point in time to the checkpoint (see column 2 lines 55-58), indicating copying contents of state memory into said CPU's internal registers and restarting said computer to the checkpoint.

However, Masubuchi fails to disclose a FIFO buffer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to use a FIFO buffer for reasons stated above.

In regards to claim 5, Official Notice is taken wherein said checkpoint controller causing said computer system to be reconfigured before restarting said computer system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to have said checkpoint controller causing said computer system to be reconfigured before restarting said computer system because applicant clearly states that it would be obvious to do so, stating that machines could be reconfigured prior to restart (see pg 9 lines 12-17 of applicant's disclosure).

In regards to claim 6, Masubuchi discloses a computer system wherein said application memory comprises fault tolerant memory. Masubuchi disclose the buffer memory for retaining the preceding state of the memory, indicating a fault tolerant memory (see figure 10 item 28 and figure 1-3 item 33 and column 1 lines 49-53).

Allowable Subject Matter

5. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Emerson Puente, whose telephone number is (703) 305-8012. The examiner can normally be reached on Monday-Friday from 8:00AM- 5:00PM, first Fridays off.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Robert Beausoliel*, can be reached on (703) 305-9713 or via e-mail addressed to [*robert.beausoliel@uspto.gov*]. The fax number for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [*emerson.puente@uspto.gov*].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 305-3900.

Emerson Puente
4/21/03


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